REMARKS

Claims 1-33, 54,55 and 58 are currently pending in the application, of which Claims 11-33, 54 and 55 stand withdrawn.

Claim Rejections - 35 U.S.C. §102

Claims 1-10 are rejected as being anticipated by Hsu (US 2003/0147277). The Examiner stated essentially that Hsu teaches all the limitations of Claims 1-10.

Claim 1 claims, *inter alia*,

> *at least one transistor having a diffusion region and a gate terminal connected directly to a write wordline; and*
>
> *a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline.*

Hsu teaches an array of non-volatile memory cells (see FIG. 4). Hsu does not teach a transistor having a diffusion region and a gate terminal connected to a write wordline; and a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor, as recited in Claim 1. FIG. 4 of Hsu illustrates an array of non-volatile memory cells, e.g., (200), including a PMOS access transistor (210) and an NMOS capacitor structure (220) (see paragraphs [0032 ~ 0033]). Hsu teaches that the two transistors (210) and (220) are commonly connected via a floating gate (216) (see FIGs. 3A, 4). The NMOS capacitor structure (220) is not connected to a diffusion region of a transistor have a diffusion region and a gate; the gate of the transistor (210) is connected to a gate of the capacitor structure (220). The gate of the transistor (210) is not connected to a wordline. Therefore, Hsu fails to teach all the limitations of Claim 1.

Therefore, for at least the above reasons, Claim 1 is patentably distinct and patentable over Hsu. Claims 2-10 are patentable over Hsu at least by virtue of their dependence from claim 1. Withdrawal of the rejection is respectfully requested.

Claims 1, 2 and 58 have been rejected under 35 USC 102(b) as being anticipated by Houghton et al. (USPN 5,757,693). The Examiner stated essentially that Houghton teaches all of the limitations of Claims 1, 2 and 58.

Claim 1 claims, inter alia, "a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline."

Houghton teaches a gain cell 20 comprising a write transistor Tw0, capacitor C0, storage node SN0, read transistor Tr0, and a diode D0 (see col. 2, lines 30-34). Houghton does not teach "a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline" as claimed in Claim 1. Houghton teaches that current is gated from BLR0 thru diode D0 and read transistor Tr0 (see FIG. 1 and col. 3, lines 10-11). The Examiner interprets the read transistor Tr0 to be a diode; respectfully, this interpretation has no support in the specification. Indeed, Houghton is clear on the metes and bounds of the term "diode", labeling the diode as D0. It is clear from FIG. 1 of Houghton that the diode D0 is connected between a bitline and a transistor. Clearly, Houghton's diode does not include a terminal connected directly to a wordline. Accordingly, Houghton fails to teach all the limitations of Claim 1.

Claims 2 and 58 depend from Claim 1. The dependent claims are believed to be allowable for at least the reasons given for Claim 1.

For the forgoing reasons, the present application, including Claims 1-33, 54,55 and 58, is believed to be in condition for allowance. Early and favorable reconsideration of the rejections is respectfully urged.

Respectfully submitted,

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